

**RB-Dfr-174**

## **8 Channel 24MHz Logic Analyser**

### **Introduction**

This is a very affordable 24Mhz 8 Channel USB Logic analyzer. This is a hobbyist level analyzer, ideal for testing your Arduino or other hobbyist microcontroller's communications. A logic analyzer is a must have tool for any serious electronics hobbyist. With a logic analyzer it is possible to see a visual representation of the zeros and ones that are flashing by between two components. A logic analyzer is different from an oscilloscope because the analyzer allows you to capture the data on a PC for a more detailed analysis of the data which is being transmitted and received. This logic analyzer supports 10 different communications standards (see Specifications below). with 8 channels it will allow you to monitor upto 8 different wires. So on an Arduino you could monitor the Serial port (tx/Rx pins), the I2C port (pins A4, A5), and the SPI port (pins 10, 11, 12, and 13) all at the same time.

### **Specifications**

8 Channels

Supports triggering (rising, high, falling, low)

Up to 24Mhz sampling

Up to 10 Billion samples

Max Voltage: 5.25Vdc

supports:

- CAN
- DMX-512
- I2C
- I2S/PCM
- Manchester
- 1-Wire
- Async Serial
- Simple Parallel
- SPI
- UNI/O
- Fully compatible with the Saleae Logic software

### **Connection diagrams**

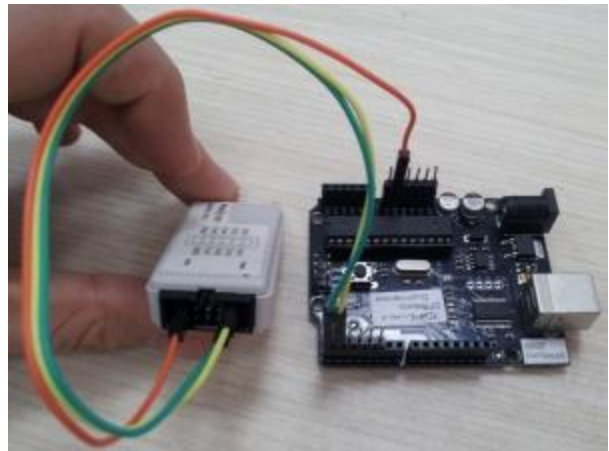
## I2C



config:



## Serial TTL



config:

Serial 2 - 'Channel 2' ▾  
Bit Rate (Bits/S) 9600  
 Use Autobaud  
8 Bits per Transfer (Standard) ▾  
1 Stop Bit (Standard) ▾  
No Parity Bit (Standard) ▾  
Least Significant Bit Sent First (Standard) ▾  
Non Inverted (Standard) ▾  
Special Mode None ▾

SPI



config:

MOSI 2 - 'Channel 2' ▾  
MISO 3 - 'Channel 3' ▾  
Clock 4 - 'Channel 4' ▾  
Enable 5 - 'Channel 5' ▾  
Most Significant Bit First (Standard) ▾  
8 Bits per Transfer (Standard) ▾  
Clock is Low when inactive (CPOL = 0) ▾  
Data is Valid on Clock Leading Edge (CPHA = 0) ▾  
Enable line is Active Low (Standard) ▾

**NOTE: It does not matter to which pin on the analyzer you connect each signal. This will be configured in the logic analyzer software later, as shown in the screen shots above.**